REMARKS/ARGUMENTS

This amendment is submitted in response to the Office Action dated July 31, 2007. Reconsideration and allowance are requested.

Claims 1, 3-11, 13-17, 19-23, and 25-41 remain in this application. Claims 2 and 18 were previously canceled. Claims 12 and 24 have been canceled by this amendment.

Formal Matters

The Applicant respectfully traverses the finality of this Office Action. In the previous office action mailed on September 6, 2006, the patentability of claims 30-38 was not addressed. The Applicant pointed this out in the response to office action dated February 2, 2007. Since this office action appears to be the first official action addressing the patentability of claims 30-38, the Applicant believes that this should be a non-final office action and respectfully requests a withdrawal of the finality of office action. In an effort to avoid abandonment, the Applicant is filing a Request for Continued Examination along with this response. **However, if the finality is withdrawn, then the Applicant requests that the fees associated with the Request for Continued Examination be refunded.**

Claim Rejection under 35 USC 102

In the Office Action, claims 1, 3-11, 14-18, 20-22 and 25-41 were rejected under 35 USC 102(b) as being anticipated by Kaneko et al. (U.S. Patent No. 6,476,463 B1). The Applicant respectfully traverses. The standard for anticipation is set forth in M.P.E.P. § 2131 as follows:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The Applicant submits that claims 1, 3-11, 14-18, 20-22 and 25-41 are patentable over Kaneko because each and every element set forth in the claims is not expressly or inherently described in Kaneko.

Claim 1

In rejecting claim 1, the Office Action asserted:

> With respect to claim 1 Kaneko et al teaches a shielded printed circuit board (PCB) (Figure 1) comprising:...a plurality of conductive vias (6) that extend from the first surface to the grounded layer (10B) so as to electrically couple the metallized polymer shield to the grounded layer (10B)...

The Applicant submits that FIG. 1 does not illustrate a (PCB) but instead a Leadless Chip Carrier (LCC) package along with a LID. The difference between a PCB and an LCC package is clearly illustrated in Kaneko's FIG. 5 which shows a PCB (31) and an LCC package (2) and their relation. Neither FIG. 1 nor FIG. 5 of Kaneko discloses "a metallized polymer shield coupled to the first surface of the PCB," as recited in the claims. Kaneko also fails to disclose "a grounded layer coupled to the second surface of the PCB." In Kaneko's FIG. 1, the grounded layer (10B) is connected to the second surface of the LCC package and not the PCB.

Kaneko also fails to disclose "a plurality of conductive vias that extend from the first surface to the grounded layer so as to electrically couple the metallized polymer shield to the grounded layer," as recited in claim 1. Although Kaneko does appear to teach two vias (6), the vias (6) does not extend from the first surface of the PCB to the grounded layer. Moreover, there is nothing to suggest that Kaneko's vias (6) is conductive. In column 5 lines 3-9, Kaneko describes the vias (6) as follows:

> The rectangular cavity 4, the microstrip antenna 5 and the through holes 6 together constitute a waveguide part 7. The waveguide part 7 has the same longitudinal and transversal dimensions as those of a tubular waveguide coupled to it. The through via holes 6 constituting the waveguide part 7 are each held in a buried fashion in the dielectric ceramic of the package substrate 3.

The description appears to suggest that the through holes or vias are hollow and therefore cannot be conductive. In order for Kaneko's through holes or vias to be conductive they must be filled with a conductive material and a lack of material or air is not sufficient o make the holes conductive. Therefore, claim 1 is patentably distinct over Kaneko under *Verdegaal* and M.P.E.P. § 2131 because Kaneko fails to disclose each and every element of claim 1.

Nevertheless, in an effort to expedite prosecution and further distinguish all the claims from the cited references, the Applicant has amended claim 1 to recite that the metallized polymer shield comprises a shaped polymer substrate that provides a cavity that is sized and shaped to receive the electronic component, wherein the shaped polymer substrate comprises a flange that extends around at least a portion of a perimeter of the cavity in a direction that is substantially parallel to the first surface of the PCB, and a metal layer disposed over at least one surface of the shaped polymer substrate. Support for this amendment can be found throughout the originally filed specification including claim 12 of the originally filed application. The Applicant respectfully requests that the Examiner reconsider the claims in light of these arguments and amendments.

Claim 4

In rejecting claim 4, the office action argued that "[w]ith respect to claim 4 with all of the limitations of claim 1, Kaneko et al teaches that the metallized polymer shield is removably coupled to the first surface of the PCB (9)." The Applicant respectfully traverses. Claim 4 depends from claim 1 and incorporates all of its limitations. For at least the same reasons as discussed above with respect to claim 1, claim 4 is also patentable over Kaneko.

Additionally, the Applicant believes that Kaneko fails to teach the metallized polymer shield is removably coupled to the first surface of the PCB. The only PCB that Kaneko describes is PCB (31), which is not connected in any way to the metallized polymer shield. It appears that the office action is calling item (9) a PCB and asserting that "the metallized polymer shield is removably coupled to the first surface of the PCB (9)." Clearly, Kaneko's item (9) is a "wiring layer" (*See column 5 line 30*), and not a PCB. One skilled in the art would not interpret a

"wiring layer" to be a PCB. Therefore, Kaneko fails to teach the metallized polymer shield is removably coupled to the first surface of the PCB, as claimed.

Claims 6 and 21

In rejecting claims 6 and 21 the Examiner argued "[w]ith respect to claims 6 and 21 and with all of the limitations of claim 5, Kaneko et al teaches that the conductive element comprises a conductive adhesive (Figure 1, element 16 i.e. a magnetic member 16 of a magnetic material, such as Fe--Ni--Co, is accommodated and secured in position by an adhesive or a solder." The Applicant respectfully traverses. Claims 6 and 21 depend from claims 1 and 15 respectively and incorporate all of their respective limitations. For at least the same reasons as discussed above with respect to claim 1 and as will be discussed below with respect to claim 15, claims 6 and 21 are also patentable over Kaneko.

Additionally, the Applicant believes that Kaneko fails to teach that the conductive elements comprise a conductive adhesive that couples the metallized polymer shield to the vias. Kaneko teaches that magnetic member 16, which is made of a magnetic material, such as Fe--Ni--Co, is accommodated and secured in position by an adhesive or a solder. However, the magnetic member is neither a metallized polymer shield nor is it secured to the vias by a conductive adhesive. Instead, according to the Office action, element 18B is the metallized polymer shield and not the magnetic member 16. Additionally, even if the magnetic member could be interpreted to be a metallized polymer shield, the magnetic member 16 is attached by an adhesive which is not necessarily a conductive adhesive and more so it is attached to the recess 13 and not the vias (6). Therefore the Applicant believes that Kaneko fails to teach that the conductive elements comprise a conductive adhesive that couples the metallized polymer shield to the vias, as claimed.

Claim 9

Claim 9 was rejected because "Kaneko et al teaches that the second surface (30) is an external, bottom surface of the PCB (32)." Clearly the grounded layer is not coupled to the second surface of the PCB. The Applicant respectfully traverses. Element 30 is not a second surface but instead a flexible connector electrode (*See Column 7 line 30 and rejection of claims 7*

and 20 of this office action). More so, FIG. 5 does not appear to teach that the PCB (31) or the mother board (32) is grounded to anything. Therefore, Kaneko does not teach that the grounded layer is coupled to the second surface of the PCB, as claimed. Additionally, because claim 9 depends from claim 1, and claim 9 is patentably distinct over Kaneko for the reasons discussed above, claim 9 is also patentable over Kaneko for those same reasons.

Claim 15

In rejection claim 15, the Office Action asserts:

> With respect to claim 15 Kaneko et al teaches a shielded printed circuit board (32) comprising: a multi-layered substrate (See figure 5) that comprises a first external surface and a second external surface, wherein a portion of the external surface is configured to receive an electronic component (Figure. 5, element 5); one or more internal grounded layers (See figure 5) disposed between adjacent layers of the multi-layered substrate (See figure 5), wherein the electrically conductive elements extend from at least one of the internal grounded planes to the first external surface; and a shield coupled (18B) to the first surface (See figure 5), the shield electrically coupled to at least some of the conductive elements to provide an electrical grounding (10b) connection between the shield and the one or more internal grounded planes (18) wherein spaces between adjacent conductive elements (20) comprise a largest dimension that is small enough to substantially reduce emission of electromagnetic radiation from the electronic component. [Column 1 paragraph 1 lines 6-10].

The Applicant respectfully traverses. Figure 5 does not illustrate a multi-layered substrate that comprises a first external surface and a second external surface, wherein a portion of the first external surface is configured to receive an electronic component. Instead, FIG. 5 illustrates a microstrip antenna (5) attached to the surface of a Leadless Chip Carrier (LCC) package. The difference between a PCB and an LCC package is clearly illustrated in Kaneko's FIG. 5 which shows a PCB (31) and an LCC package (2) and their relation. Additionally, neither FIG. 1 nor FIG. 5 of Kaneko discloses "a shield coupled to the first surface, the shield electrically coupled to at least some of the conductive elements to provide an electrical grounding connection between the shield and the one or more internal grounded planes," as

recited in claim 15. In Kaneko's FIG. 1 and FIG. 5, the grounded layer (10B) is connected to the second surface of the LCC package and not the PCB. Therefore, claim 15 is patentably distinct over Kaneko under *Verdegaal* and M.P.E.P. § 2131 because Kaneko fails to disclose each and every element of claim 1.

Nevertheless, in an effort to expedite prosecution and further distinguish all the claims from the cited references, the Applicant has amended claim 15 to recite that the shield comprises a shaped polymer substrate that provides a cavity that is sized and shaped to receive an electronic component, wherein the shaped polymer substrate comprises a flange that extends around at least a portion of a perimeter of the cavity in a direction that is substantially parallel to the first external surface of the PCB, and a metal layer disposed over at least one surface of the shaped polymer substrate. Support for this amendment can be found throughout the originally filed specification including claim 24 of the originally filed application. The Applicant respectfully requests that the Examiner reconsider the claims in light of these arguments and amendments.

Claim 30

In rejection claim 30, the Office Action asserted:

> With respect to claim 30 Kaneko et al teaches a method of shielding an electronic component on a printed circuit board (PCB), the method comprising:...a plurality of conductive vias (6) that extend from the coupling of a metallized polymer shield to the first surface of the PCB (32) and around the electronic component to create an electrical connection to the conductive vias and the grounded layer (10B) wherein the electrical connection between the grounded layer(s), vias. and the metallized polymer shield forms a grounded EMI shield that substantially surrounds the electronic component (14)...

The Applicant submits that neither FIG. 1 nor FIG. 5 illustrates a method of shielding an electronic component on a printed circuit board (PCB) but instead a method of attaching a Leadless Chip Carrier (LCC) package along with a LID to a motherboard. Figure 1 of Kaneko illustrates details of an LCC package but not a PCB whereas FIG. 5 of Kaneko illustrates how the LCC can be attached to a motherboard.

Kaneko also fails to disclose that the "electrical connection between the grounded layer(s), vias, and the metallized polymer shield forms a grounded EMI shield that substantially surrounds the electronic component" as recited in claim 30. Although Kaneko does appear to teach two vias (6), Kaneko's vias (6) are not conductive because they are holes are hollow with no filling, as explained earlier with reference to claim 1. Since the vias (6) are not conductive, the electrical connection between the grounded layer(s), vias, and the metallized polymer shield can not form a grounded EMI shield that substantially surrounds the electronic component, as recited in claim 30. Therefore, claim 30 is patentably distinct over Kaneko under *Verdegaal* and M.P.E.P. § 2131 because Kaneko fails to disclose each and every element of claim 30.

Nevertheless, in an effort to expedite prosecution and further distinguish all the claims from the cited references, the Applicant has amended claim 30 to recite that the metallized polymer shield comprises a shaped polymer substrate that provides a cavity that is sized and shaped to receive the electronic component, wherein the shaped polymer substrate comprises a flange that extends around at least a portion of a perimeter of the cavity in a direction that is substantially parallel to the first surface of the PCB, and a metal layer disposed over at least one surface of the shaped polymer substrate. Support for this amendment can be found throughout the originally filed specification including claims 12 and 24 of the originally filed application. The Applicant respectfully requests that the Examiner reconsider the claims in light of these arguments and amendments.

Claims 3, 5, 7, 8, 10-11, 14, 16-17, 20, 22, 25-29, 31-41

Claims 3, 5, 7, 8, 10-11, 14, 16-17, 20, 22, 25-29 and 31-41 depend from claims 1, 15 and 30 respectively and incorporate all of their respective limitations. For at least the same reasons as discussed above with respect to claims 1, 15 and 30, claims 3, 5, 7, 8, 10-11, 14, 16-17, 20, 22, 25-29 and 31-41 are also patentable over Kaneko.

Claim Rejection under 35 USC 103

In the Office Action, claims 12, 13, 23, and 24 were rejected under 35 USC 103(a) as being unpatentable over Higgins. The Applicant respectfully traverses.

Although claims 12 and 24 have been canceled, the limitations have been incorporated into claims 1 and 15, respectively. Therefore, the patentability of claims 12 and 24 is addressed herein.

In rejecting claims 12 and 24, the Office Action first asserted that Higgins teaches all of the limitations of claims 1 and 15 except "that a metal layer is disposed over at least one surface of the shaped polymer substrate." The Office Action then rejected the claims by asserting that "it would have been obvious to one of ordinary skill in the art at the time of the invention [to] add a metal layer disposed on a surface of the shaped polymer substrate for the purpose of adding structural strength while increasing the shielding capability of the structure."

The Applicant respectfully disagrees with both of these rejections because they are dependent on the rejection of their respective base claims under 35 USC 102(b). This Office Action has not explained why Higgins teaches each and every element of the independent claims. In the previous Office Action, the same rejection was given but the claims were amended and arguments for patentability provided. For those same reasons articulated in the previous response to Office Action, claims 12 and 24 are patentable over Higgins. If the Office Action intended to use Kaneko as the reference in this rejection, instead of Higgins, then the Applicant also submits that claims 12 and 24 are patentable over Kaneko. Since claims 12 and 24 depend from claims 1 and 15 respectively and incorporate all of their respective limitations, claims 12 and 24 are also patentable over Kaneko for at least the same reasons as discussed above with respect to claims 1 and 15. Similarly, since claims 13 and 23 depend from claims 1 and 15 respectively and incorporate all of their respective limitations, claims 13 and 23 are also patentable over Kaneko for at least the same reasons as discussed above with respect to claims 1 and 15.

In the Office Action, the Examiner rejected claim 19 under 35 USC 103(a), as being unpatentable over Higgins in view of Kaneko (US Patent 6476463). The Office Action acknowledged that Higgins "does not specifically teach that the largest dimension is smaller than half a wavelength of EMI emissions from the electronic component. Kaneko teaches vias that are separated by certain dimension wherein the largest dimension is smaller than half a wavelength of EMI emissions from the electronic component (column 5, lines 13-17). It would

have been obvious to one of ordinary skill in the art at the time of the invention to have the largest dimension separating vias to be smaller than half a wavelength of EMI emissions from the electronic component, for the purpose of quickly attenuating the EMI emissions."

As explained in the previous response to Office Action, although Kaneko does teach spacing apart the through holes 6 at an interval that is sufficiently small compared to one half the wavelength of an electromagnetic wave guided by the waveguide, one skilled in the art would not have been motivated to modify Higgins to use Kaneko to make the claimed invention. The claimed invention adjusts the spaces between adjacent conductive elements to be the largest dimension that is small enough to substantially reduce emission of electromagnetic radiation from the electronic component. Clearly, Kaneko is adjusting the spacing to prevent energy loss in the waveguide and not to reduce emission of electromagnetic radiation from the electronic component.

Additionally, claim 19 depends from claim 15 and incorporates all of its respective limitations. For at least the same reasons discussed above with respect to claim 15, claim 19 does not teach or suggest all of the claimed limitations.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance and an action to that end is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,

/Jesus Del Castillo/

Jesus Del Castillo
Reg. No. 51,604

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor, San Francisco, CA 94111-3834
Tel: 650-326-2400 / Fax: 415-576-0300
JDC:gjs

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